WHAT IS CLAIMED IS:

1. A semiconductor package comprising:

a plurality of leads, each of the leads defining:

a first surface;

a second surface disposed in opposed relation to the first surface; and

a third surface disposed in opposed relation to the second surface and laterally offset outwardly relative to the first surface;

a first semiconductor die defining opposed top and bottom surfaces;

a second semiconductor die defining opposed top and bottom surfaces;

a plurality of conductive connectors electrically and mechanically connecting the first semiconductor die to the first surfaces of the leads and the second semiconductor die to the second surfaces of the leads; and

an encapsulating portion applied to and at least partially encapsulating the leads, the first and second semiconductor dies, and the conductive connectors.

2. The semiconductor package of Claim 1 wherein the conductive connectors each comprise a conductive bump.

3. The semiconductor package of Claim 2 wherein the conductive bump is fabricated from material selected from the group consisting of:

gold; and

solder.

4. The semiconductor package of Claim 1 wherein:

the first semiconductor die includes a plurality of bond pads disposed on the top surface thereof;

the second semiconductor die includes a plurality of bond pads disposed on the bottom surface thereof;

and

the conductive connectors are used to electrically and mechanically connect the bond pads of the first semiconductor die to respective ones of the first surfaces of the leads and the bond pads of the second semiconductor die to respective ones of the second surfaces of the leads.

5. The semiconductor package of Claim 4 wherein the conductive connectors each comprise a conductive bump.

6. The semiconductor package of Claim 1 wherein:

each of the leads includes a first bump land formed at a prescribed region of the first surface thereof and a second bump land formed at a prescribed region of the second surface thereof;

the conductive connectors each comprise a conductive bump; and

the conductive bumps are fused to respective ones of the first and second bump lands of each of the leads.

7. The semiconductor package of Claim 6 wherein each of the leads includes:

a first protective layer formed on at least a portion of the first surface thereof other than for the prescribed region including the first bump land; and

a second protective layer formed on at least a portion of the second surface thereof other than for the prescribed region including the second bump land.

8. The semiconductor package of Claim 7 wherein the protective layer is selected from the group consisting of:

a polyimide;

titanium;

aluminum; and

a solder resist.

9. The semiconductor package of Claim 1 wherein each

of the leads includes:

a first protective layer coated on the first surface thereof about a respective one of the conductive connectors; and

a second protective layer coated on the second surface thereof about a respective one of the conductive connectors.

10. The semiconductor package of Claim 9 wherein the protective layer is selected from the group consisting of:

a polyimide;

titanium;

aluminum; and

a solder resist.

11. The semiconductor package of Claim 1 wherein the first and second semiconductor dies are identically sized.

12. The semiconductor package of Claim 1 wherein the encapsulating portion is applied to the leads such that the third surface of each of the leads is exposed within the encapsulating portion.

13. The semiconductor package of Claim 12 wherein the encapsulating portion is applied to the first and second semiconductor dies such that the bottom surface of the first semiconductor die and the top surface of the second semiconductor die are each exposed within the encapsulating portion.

14. The semiconductor package of Claim 13 wherein the leads and first semiconductor die are oriented relative to each other such that the bottom surface of the first semiconductor die is substantially flush with the third surface of each of the leads.

15. The semiconductor package of Claim 12 wherein:

each of the leads further defines an outer end which extends between the second and third surfaces thereof; and

the encapsulating portion is applied to the leads

such that the outer end of each of the leads is exposed within the encapsulating portion.

16. The semiconductor package of Claim 1 wherein each of the leads further defines a fourth surface disposed in opposed relation to the third surface and laterally offset outwardly relative to the second surface.

17. The semiconductor package of Claim 16 wherein the encapsulating portion is applied to the leads such that the third and fourth surfaces of each of the leads are exposed within the encapsulating portion.

18. The semiconductor package of Claim 17 wherein the encapsulating portion is applied to the first and second semiconductor dies such that the bottom surface of the first semiconductor die and the top surface of the second semiconductor die are each exposed within the encapsulating portion.

19. The semiconductor package of Claim 18 wherein the second semiconductor die and the leads are oriented relative to each other such that the top surface of the second semiconductor die is substantially flush with the fourth surface of each of the leads.

20. The semiconductor package of Claim 19 wherein the first semiconductor die and the leads are oriented relative to each other such that the bottom surface of the first semiconductor die is substantially flush with the third surface of each of the leads.

21. The semiconductor package of Claim 17 further in combination with a second semiconductor package identically configured to the semiconductor package, the third surfaces of the leads of the second semiconductor package being electrically connected to respective ones of the fourth surfaces of the leads of the semiconductor package.

22. A method of fabricating a semiconductor package, comprising the steps of:

a) providing a plurality of leads, each of the

leads having a first surface, a second surface disposed in opposed relation to the first surface, and a third surface disposed in opposed relation to the second surface and laterally offset outwardly relative to the first surface;

b) electrically and mechanically connecting a first semiconductor die to the first surface of each of the leads;

c) electrically and mechanically connecting a second semiconductor die to the second surface of each of the leads; and

d) applying an encapsulant to the first and second semiconductor dies and the leads to form an encapsulating portion which at least partially encapsulates the first and second semiconductor dies and the leads.

23. The method of Claim 22 wherein the first and second semiconductor dies each include a plurality of bond pads, and:

step (b) comprises electrically and mechanically connecting the bond pads of the first semiconductor die to respective ones of the first surfaces of the leads through the use of conductive bumps; and

step (c) comprises electrically and mechanically connecting the bond pads of the second semiconductor die to respective ones of the second surfaces of the leads through the use of conductive bumps.

24. The method of Claim 22 wherein step (d) comprises applying the encapsulant to the leads such that the third surface of each of the leads is exposed within the encapsulating portion.

25. The method of Claim 21 wherein:

step (a) further comprises providing each of the leads with a fourth surface which is disposed in opposed relation to the third surface and laterally

offset outwardly relative to the second surface; and

step (d) comprises applying the encapsulant to the leads such that the third and fourth surfaces of each of the leads are exposed within the encapsulating portion.

26. The method of Claim 25 further comprising the step of:

e) electrically and mechanically connecting the third surfaces of the semiconductor package to respective ones of the fourth surfaces of another identically configured semiconductor package.